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Ageing behaviour of electrochemical double layer capacitors Part II. Lifetime simulation model for dynamic applications

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Abstract

Based on the results of the experimental study in Part I [1], a holistic simulation model that combines electrical and thermal simulation of electrochemical double-layer capacitor (EDLC) modules with an ageing model is presented. This simulation model allows analysing self-accelerating degradation effects caused by elevated voltages and temperatures. Furthermore, the divergence of cell performance in a stack of cells can be investigated which makes the model a valuable tool for cell and stack design as well as for testing operating strategies and cooling systems.

Keywords: Electrochemical double layer capacitor (EDLC); Supercapacitor; Ageing; Electrochemical impedance spectroscopy (EIS); State of health (SOH)

1. Introduction

Electrochemical double layer capacitors (EDLCs) are storage devices with a high power density and high robustness compared to most battery technologies and are therefore an interesting option for automotive applications [2].

With respect to robustness especially their high cycle life is a key advantage, since it allows to design the storage module for the lifetime of the complete system, unlike most battery technologies [3,4].

Yet, EDLCs are sensitive to ageing processes and can only meet the requirements on life expectancy if certain boundary conditions – especially with respect to temperature and voltage – are met. In Part I [1], the influence of temperature and voltage on the ageing behaviour of EDLCs was experimentally analysed and based on the results a heuristic ageing model was developed.

In a storage system temperature and voltage are however not only an external influence but are significantly affected by the devices themselves and the operating mode. Hence, in this paper a holistic simulation model is presented, that combines the ageing model with electric and thermal models of the devices and the energy storage system in order to study mutual influences and feedback effects on a system level.

2. Simulation of EDLC ageing

A holistic ageing model was implemented in Matlab/Simulink in order to analyse the effects of different system designs and operating conditions on ageing and performance of EDLCs. The model consists of an electrical model, which allows to determine the cell voltages and the internal power losses for a given current profile, a thermal model that calculates the spatial temperature distribution in an EDLC stack and an ageing model, which determines the changes of the impedance model parameters. The feedback of the changed parameters into the electrical model allows modelling self-accelerating ageing effects, which is a key feature of the model.

2.1. Electrical model

The electrical simulation model is a lumped-element impedance model, as shown in Fig. 1. The element R_s corresponds to the series resistance caused by the metallic conductors and the electrolyte, L_s is the series inductance which is mainly influenced by the geometry of the electrodes and connectors and $\underline{Z}_p$ models the complex pore impedance that is typical for double layer capacitors. The complete impedance model for an EDLC

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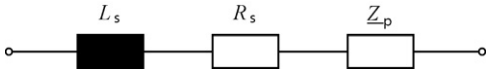

Fig. 1. Equivalent circuit of an EDLC.

including series resistance and inductance can be expressed in a closed expression:

$$Z_{\mathrm{EDLC}} = R_{\mathrm{s}} + \mathrm{j}\omega L_{\mathrm{s}} + \underline{Z}_{\mathrm{p}}. \tag{1}$$

A standard model of the pore impedance described by several authors [5–7] is

$$Z_{\mathrm{ps}} = \sqrt{\frac{R_{\mathrm{el}}}{\mathrm{j}\omega C_{\mathrm{dl}}}} \cdot \coth\sqrt{\mathrm{j}\omega R_{\mathrm{el}} C_{\mathrm{dl}}}, \tag{2}$$

where R_{el} is the resistance of the electrolyte in the pores and C_{dl} is the double layer capacitance. This model however fails to describe the low frequency behaviour of EDLCs adequately, therefore an improved model of a generalised pore impedance was described in Part I [1]:

$$Z_{\mathrm{pg}} = \sqrt{\frac{R_{\mathrm{el}}}{(\mathrm{j}\omega)^{\gamma} A_{\mathrm{dl}}}} \cdot \coth\sqrt{(\mathrm{j}\omega)^{\gamma} R_{\mathrm{el}} A_{\mathrm{dl}}}. \tag{3}$$

The standard model was extended by a constant phase element, where A_{dl} formally replaces the double layer capacitance and the exponent γ is closely related to the phase angle of the impedance. The difference between the models is mainly relevant in the low frequency region. Comparing the low frequency approximation of the standard model

$$Z_{\mathrm{ps}}(\omega \to 0) \approx \frac{R_{\mathrm{el}}}{3} + \frac{1}{\mathrm{j}\omega C_{\mathrm{dl}}}, \tag{4}$$

with that of the generalised model

$$Z_{\mathrm{pg}}(\omega \to 0) \approx \frac{R_{\mathrm{el}}}{3} + \frac{1}{(\mathrm{j}\omega)^{\gamma} A_{\mathrm{dl}}}. \tag{5}$$

shows that for $\gamma < 1$ the generalised pore impedance has a resistive component that increases with decreasing frequency, while the standard model passes into purely capacitive behaviour.

The standard pore impedance Z_{ps} can be derived from an infinite ladder network of infinitesimal resistors and capacitors (cf. Part I [1] and [8]), consequently, it can be approximated by a ladder network with a finite number of elements. For a network with N elements of each type the corresponding elements can formally be calculated as $R'_{\mathrm{el}} = R_{\mathrm{el}}/N$ and $C'_{\mathrm{dl}} = C_{\mathrm{dl}}/N$, respectively.

Linzen [6] proposed a modified ladder-network which yields a much better approximation for small numbers of elements. The first resistor is removed from the ladder network and the remaining resistance elements are multiplied by an empiric correction factor $\alpha(N)$, i.e. $R'_{\mathrm{el},\alpha} = \alpha(N) \cdot R_{\mathrm{el}}/N$. Fig. 2 shows this modified ladder network. For the simulations presented in this paper a ladder network with $N = 10$ and a correction factor of $\alpha = 1.17$ was used.

Unfortunately, there is no accurate model for the generalised pore impedance Z_{pg} (cf. Eq. (3)) which can be implemented

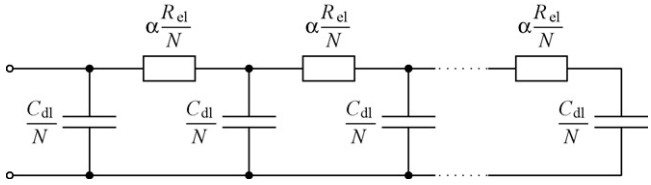

Fig. 2. Optimised electric circuit model of the standard pore impedance Z_{ps}.

likewise effectively with respect to computation time. In principle, the desired behaviour can be accomplished by branched ladder networks, yet for a CPE exponent close to one a high degree of branching would be required [9] which would lead to large networks and consequently poor computational efficiency.

A different approach for a time-domain model of CPE behaviour proposed in ref. [6] is the convolution of the current signal with the inverse Laplace transform of the CPE element. Again, the drawback of this implementation is the necessary computational effort since the convolution operation includes the complete time series of the signal, or – for a practical implementation – at least a relevant part of it.

For a holistic model, fast computation time is essential since several EDLCs in a stack have to be calculated in parallel and the simulation has to cover long time periods. A good compromise between high model accuracy in the relevant frequency range and high computational efficiency could be accomplished by adding a single parallel RC circuit in series with the ladder network that represents the standard pore impedance, as shown in Fig. 3. The main effect of this RC-circuit is a contribution to the real part of the impedance for low frequencies. This model extension does not provide CPE behaviour for $\omega \to 0$, but is effective only in a limited frequency range. The model parameters can be calculated directly from the impedance parameters A_{dl} and γ by equating the real part of the RC-circuit at its characteristic angular frequency ω_x with the difference of the real parts of the standard and the general pore model. Using the low frequency approximations given in Eqs. (4) and (5) the difference of the two models equals the real part of the CPE branch:

$$\Re(Z_{\mathrm{pg}} - Z_{\mathrm{p}}) \approx \Re\left(\frac{1}{(\mathrm{j}\omega)^{\gamma} A_{\mathrm{dl}}}\right) = \frac{\cos(\gamma\pi/2)}{\omega^{\gamma} A_{\mathrm{dl}}}. \tag{6}$$

Taking into account that the real part of the impedance of a parallel RC circuit at its characteristic frequency $\omega_x = R_x C_x$ is $R_x/2$, the resistance R_x and capacitance C_x can be calculated as

$$R_x = \frac{2\cos(\gamma\pi/2)}{\omega_x^{\gamma} A_{\mathrm{dl}}} \quad \text{and} \quad C_x = \frac{1}{\omega_x R_x}. \tag{7}$$

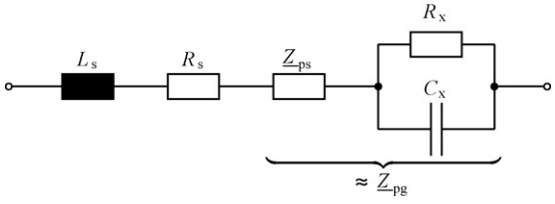

Fig. 3. Equivalent circuit of the simulation model; the generalised pore impedance Z_{pg} is approximated by a standard pore impedance Z_{ps} and a parallel RC-circuit (R_x, C_x).

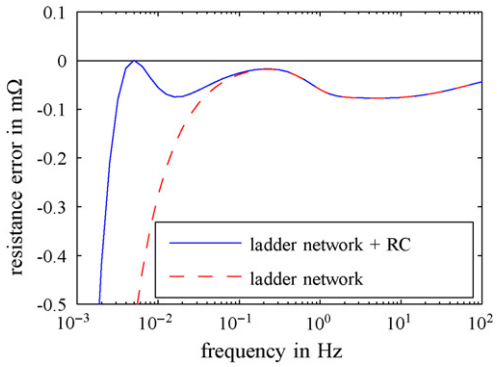

Fig. 4. Difference of the real part of the impedance between the finite ladder network with and without additional RC-circuit and the true pore impedance according to Eq. (3) for typical impedance parameters (R_s=0.34 m Ω, R_{el}=1.77 m Ω, A_{dl}=729 $F_s^{(\gamma-1)}$, γ=0.992) (cf. Part I [1]).

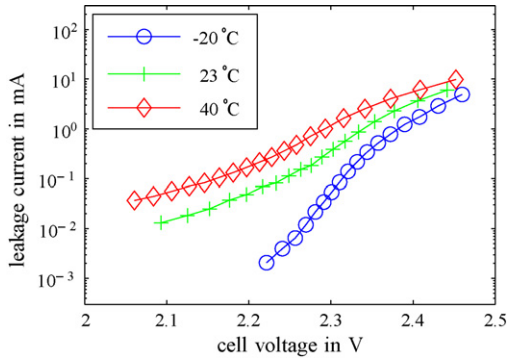

Fig. 5. Self-discharge current determined for commercial EDLCs (Maxwell, 350 F/2.5 V, purchased in 2004 [12]) at different temperatures according to Eq. (8).

The angular frequency ω_x can be freely chosen, yet it has to be significantly smaller than the characteristic frequency of the pore impedance ($\omega_x \ll R_{el}A_{dl}$) in order to restrict the influence to the low frequency branch. For the simulation $\omega_x = 2\pi\cdot 5$ mHz was chosen.

Fig. 4 illustrates the effect of the additional RC circuit on the real part of the impedance, which determines the power losses inside the EDLC. The error in the range between 5 and 50 mHz could be significantly reduced, the model error at very low frequencies has very few influence on the simulation, since the spectrum of the current contains virtually no power at frequencies below 5 mHz. For frequencies above 100 mHz both models show identical results, the remaining difference compared to the true pore impedance is due to the limited elements of the finite ladder network used for the simulation. The accuracy of the model could be further improved by using more elements in the ladder network and additional RC-circuits, however at the cost of simulation speed.

The model parameters depend on cell temperature and voltage, the latter introducing non-linearity to the model [7]. Voltage and temperature dependencies of the impedance parameters were determined by measurements and are stored in lookup tables.

2.2. Self-discharge

Self-discharge of EDLCs is a very slow process, that cannot be adequately determined by impedance measurements. Instead, the progression of the open circuit voltage (OCV) after a full charge of the EDLC can be analysed, which shows a quasi-exponential decrease. The time constant of this discharge depends not only on several parameters, first of all temperature, but also on the initial open circuit potential, and changes significantly during the first hours [10,11].

If the capacitance of the EDLC is known, the leakage current as a function of voltage can be calculated from the slope of the voltage curve:

$$i_{leak} = -C_{dl}\frac{dU}{dt}. \tag{8}$$

The underlying assumption is that for time constants in the range of hours and days the pore impedance can be modelled as an ideal capacitor (cf. Eq. (4)).

Fig. 5 shows a semi-logarithmic plot of the leakage current determined at three different temperatures for a commercial EDLC. The strong variation of the leakage current over more than two decades in a small voltage window makes clear, that self-discharge cannot be adequately modelled by a linear parallel resistor but shows approximately an exponential behaviour. A measured self-discharge characteristic can be introduced in an impedance model as a voltage dependent current source, which corresponds to a non-linear resistor, in parallel to the pore impedance.

EDLCs in series connection are virtually never used without a voltage balancing system. A basic passive cell balancing comprised of a 100 Ω resistor in parallel to each cell was therefore included in the system model. Self-discharge is yet not explicitly included in the simulation model, since leakage currents can be neglected compared to the current of the balancing system.

2.3. Thermal model

The thermal model is divided into two submodels, heat generation and heat dissipation. Heat generation in double layer capacitors comprises two parts, Joule heat and reversible heat [13]. The Joule heat dQ_{Joule}/dt results directly from the ohmic losses of the EDLC which can be derived from the electric equivalent circuit [6]:

$$\frac{dQ_{Joule}(t)}{dt} = P_{Loss} = i^2(t)R_s + \sum_{k=1}^{N-1} i_k^2(t)R'_{el,\alpha} + i_x^2(t)R_x \tag{9}$$

where $i(t)$ is the applied current, R_s the series resistance, $R'_{el,\alpha}$ the resistance of one element of the equivalent ladder circuit, i_k the current through the resistance of the kth ladder element and $i_x(t)$ is the current through R_x.

The reversible heat results from entropy changes due to the ion movement in the electrolyte. It is calculated as

$$\frac{dQ_{rev}(t)}{dt} = 2\frac{Tka}{e}i(t) \tag{10}$$

where T is the absolute temperature, $k = 1.380658 \times 10^{-23}$ J<CE:HSP SP="0.25"/> K^{-1} the Boltzmann constant, a a factor depending on the geometry of the double layer capacitor, $e = 1.602176 \times 10^{-19}$ C the elementary charge and $i(t)$ is the current.

Joule heat and reversible heat are calculated for each cell individually to be able to consider different resistance and capacitance evolutions for each cell, which influence the heat generation.

For the heat dissipation model, each cell is divided into small volume elements [6,14]. Each of these elements has a heat capacitance and exchanges heat with its neighbour elements via thermal resistances. Neighbour elements can be located in the same cell, other cells or in the environment, which is used to model convection and radiation. Input data needed by the heat dissipation model are geometric data and material data of the cell. Different stack and environment configurations can be set, such as the number of cells, their electrical connections, the initial temperature of the stack and the temperature of surrounding objects. More details about the thermal model can be found in refs. [13,14].

2.4. Ageing model

An ageing model that describes the changes of the parameters of the impedance model has been derived from extensive measurements on different types of EDLCs during accelerated ageing tests and is described in Part I [1].

The ageing model calculates the equivalent ageing time according to equation

$$t_{\mathrm{eq}} = t \cdot c_T^{(T-T_0)/\Delta T} \cdot c_V^{(V-V_0)/\Delta V} \tag{11}$$

based on the voltage V and average temperature T of each individual cell.

The constants T_0, V_0, ΔT and ΔV can be chosen arbitrarily as reference points for the ageing model, c_{T} and c_{V} are model parameters that have to be determined experimentally for the respective device, as described in Part I [1].

Consequently, the cells have different equivalent ages, depending on the thermal and voltage stress they have experienced. From the equivalent ageing time, the parameters of the impedance model are calculated according to

$$a(t, T, V) = a_{\mathrm{init}} \cdot \left(1 + c_{\mathrm{a}} \cdot t_{\mathrm{eq}}\right), \tag{12}$$

where a stands for one of the impedance model parameters R_{s}, R_{el}, A_{dl} and γ. Typical parameters for different types of devices are presented in Part I [1].

It should be noted, that the ageing model makes use of some assumptions and simplifications that have not been experimentally proven yet:

- Ageing due to voltage and thermal stress is assumed to be the predominant process, other processes are not covered by the model.
- The exponential dependency on temperature and voltage that was experimentally verified for elevated voltages and temperatures is extrapolated towards voltages and temperatures below the rated values V_{r} and T_{r}.
- The relative change of an impedance parameter after a certain ageing time is assumed to be constant, irrespective of the current temperature and voltage. For example, if the capacitance decreased by 10% due to ageing, this relative change would be applied to the capacitance at 20° C and 2.0 V as well as at 40° C and 2.5 V.

These assumptions lead to reasonable results in most cases, however it is clear, that larger the model uncertainty the more the simulated conditions differ from the experimental conditions.

2.5. Holistic model and simulation setup

The holistic simulation model combines the electrical, thermal and ageing model. The electrical and thermal models are directly coupled, i.e. voltage and temperature are calculated at each time step and the impedance parameters are immediately updated accordingly. A real time simulation of several years is currently not possible in reasonable simulation time. The simulation is therefore split into simulation periods of a few hours with a realistic load profile. The ageing model is only updated after each simulation period. From a given current profile, the resulting voltage and temperature curves are calculated, and based on these curves, the equivalent ageing time t_{eq} according to Eq. (11) is calculated.

Now the impact on the resistances and the capacitance can be calculated according to Eq. (12); parameters of the ageing model are presented in Part I [1]. The updated values are then used in the next simulation. Fig. 6 shows the sequence of the whole simulation.

As an example, a stack of 12 prismatic cells (Nesscap 600 F [15]), electrically connected in series (see Fig. 7), has been simulated. The cells are arranged directly side by side and the initial temperature of the cells is 40 °C. On one side of the stack, there is a hot wall (60 °C) which could represent a close-by combustion engine, the temperature of all other surroundings is 40 °C.

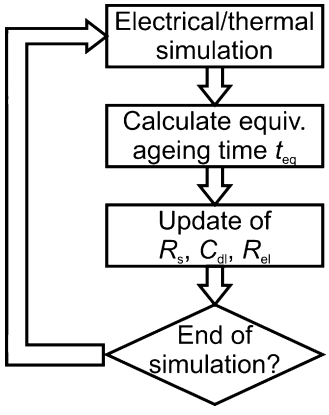

Fig. 6. Simulation sequence consisting of electrical/thermal simulation and parameter update because of ageing.

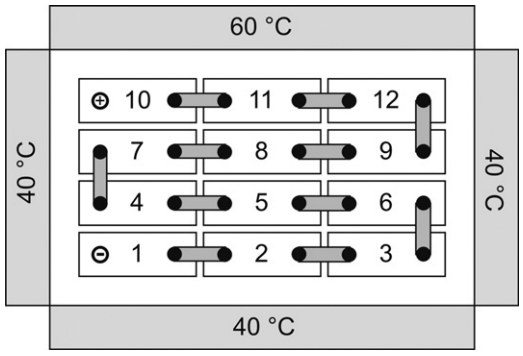

Fig. 7. Stack design for the ageing simulation. The blocks around the stack symbolise objects in the surroundings and their temperature.

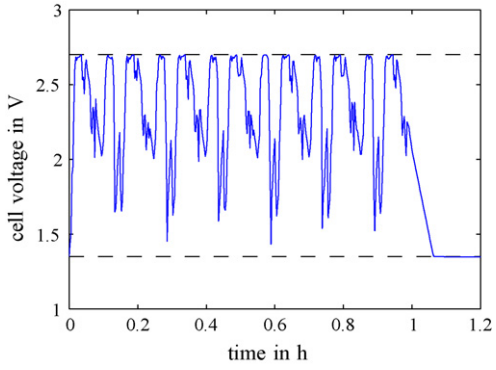

Fig. 8. Cell voltage produced by the impedance model.

The current profile used for the simulation results presented here was derived from measurements on a hybrid electric car and covers a current range of about ±100 A. The basic sequence of approximately 10 min has been concatenated to a drive cycle of 1 h. In a system such as a hybrid electric vehicle the voltage of the stack is controlled by the energy management and the controller of the power converter. A voltage control is therefore included in the simulation model. The controller limits the voltage for the whole stack to be between 32.4 V and 16.2 V, which corresponds to a voltage per cell of 2.7 V (V_r) and 1.35 V ($0.5V_r$), respectively, indicated by the dashed lines in Fig. 8. The voltage controller reduces the charging current as soon as the upper or lower voltage limit is reached. The individual cell voltages however disperse as soon as the properties of the cells – first of all the capacitances – vary due to different ageing stress. During one simulation period, the current profile is applied for the first hour followed by a discharge with 2 A to $V_r/2$=1.35 V per cell and a rest period of approximately 2 h. The resulting temperature pattern is displayed in Fig. 9 for a stack that has already endured a simulated service time of 7 years. While the current profile is applied, the cells heat up. The cells adjacent to the hot wall (cells 10–12) are additionally heated and thus reach the highest temperatures. During the discharge and rest period the cells cool down slowly by dissipating their heat to the environment.[1]

[1] The effect of cooling during a discharge with a moderate current is explained in detail in ref. [13].

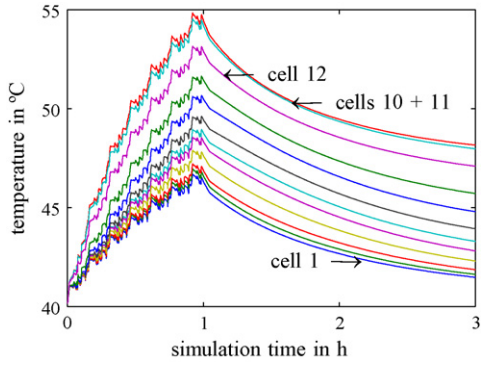

Fig. 9. Cell temperatures during the simulation for a stack with aged cells after 7 years simulated service time.

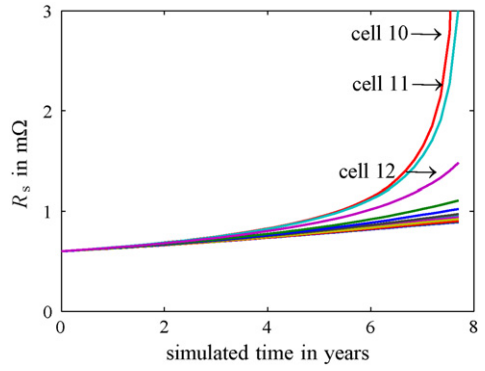

Fig. 10. Evolution of the series resistance R_s for each cell.

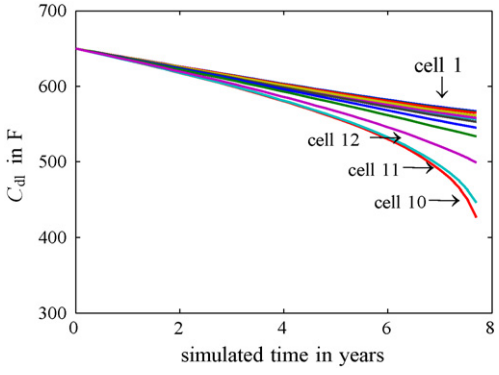

Fig. 11. Evolution of the double layer capacitance C_{dl} for each cell.

2.6. Simulation results

Figs. 10 and 11 show the evolution of the series resistance R_s and the capacitance C_{dl}, respectively, for all cells over the complete simulation cycle.[2] Cells 10–12 show a quasi-exponential change of these factors towards the end of the simulation, while most of the cells have a moderate and nearly linear increase and

[2] Both R_s and the capacitance C_{dl} vary slightly with temperature and voltage; Figs. 10 and 11 show values that correspond to the average voltage and temperature level during the simulation. The development of the pore resistance R_{el} is qualitatively the same as of the series resistance R_s and is therefore not discussed further.

cell #10 R_s = 1.51 mΩ C_{dl} = 497 F	cell #11 R_s = 1.44 mΩ C_{dl} = 502 F	cell #12 R_s = 1.18 mΩ C_{dl} = 525 F
cell #7 R_s = 0.92 mΩ C_{dl} = 562 F	cell #8 R_s = 0.95 mΩ C_{dl} = 556 F	cell #9 R_s = 1.01 mΩ C_{dl} = 548 F
cell #4 R_s = 0.90 mΩ C_{dl} = 565 F	cell #5 R_s = 0.89 mΩ C_{dl} = 566 F	cell #6 R_s = 0.88 mΩ C_{dl} = 569 F
cell #1 R_s = 0.86 mΩ C_{dl} = 574 F	cell #2 R_s = 0.86 mΩ C_{dl} = 573 F	cell #3 R_s = 0.87 mΩ C_{dl} = 572 F

Fig. 12. Distribution of R_s and C_{dl} in the EDLC stack after 7 years simulated service time. Shading indicates the grade of deterioration.

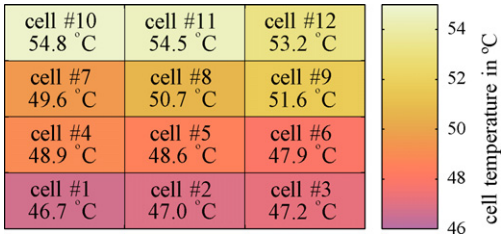

Fig. 13. Temperature distribution in the module after 7 years simulated service time.

decrease of their internal resistance and capacitance, respectively.

The reasons for this strong dispersion are two self-accelerating effects. Firstly, the temperature of these cells becomes higher because they are close to the hot wall (cf. Fig. 7), which increases their ageing process and consequently their series and pore resistance increases, too. A higher resistance leads to a stronger self-heating of the cell, thus to accelerated ageing and so on. Secondly, during ageing the capacitance of the cell decreases, so during charging the cell with the lowest capacitance reaches the highest voltage. Since only the stack voltage is controlled and the passive cell balancing is relatively slow, the "oldest" cells have the lowest capacitances and the highest charging voltages which again leads to accelerated ageing.

The strong influence of inhomogeneous temperature in a stack becomes clear by comparing Figs. 12 and 13. Fig. 12 depicts the distribution of the series resistance R_s and capacitance C_{dl} values in the cells after 7 years simulated operating time. Fig. 13 shows the distribution of the maximum temperature reached in each of the cells during one drive cycle.

Cells 10–12, which are close to the hot wall, show higher temperatures than the other cells[3] and also the strongest degradation. The inhomogeneous temperature induced by the hot wall is the cause for the different ageing rates of the cells, the strong exponential ageing behaviour can however only be understood by the self-accelerating nature of the process. A simulation that disregards this positive feedback component would significantly overestimate the life expectancy of the EDLCs.

[3] Cell 12 has a lower temperature than cell 11 since the electric connector to cell 9 allows a better heat exchange with the cooler cell.

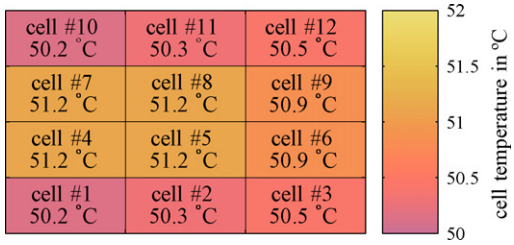

Fig. 14. Temperature distribution in the module for stack B prior to ageing.

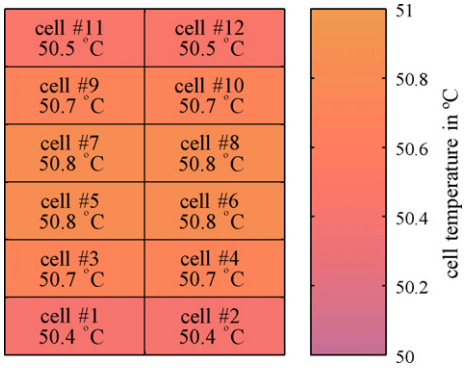

Fig. 15. Temperature distribution in the module for stack A prior to ageing.

2.7. Application example

Besides simulation of the self-accelerating effects of EDLC ageing, the holistic model can be used for the optimisation of operating strategies and stack design. As an example, two different stack designs have been compared with respect to their ageing behaviour. Stack A is identical to the stack shown in Fig. 7, except that the ambient temperature has been set to 45 °C for all sides of the stack. Stack B has the same number of cells connected in series, but the cells are arranged in two lines of six cells each. The ambient temperatures, voltage limits and current profiles are identical for both stacks in order to compare only the influence of the arrangement of the cells.

Figs. 14 and 15 show the maximum temperature in the cells of both stacks during the first simulation cycle, i.e. with fresh cells. Though the temperature differences between the cells are small due to the homogeneous ambient temperature, it can be seen

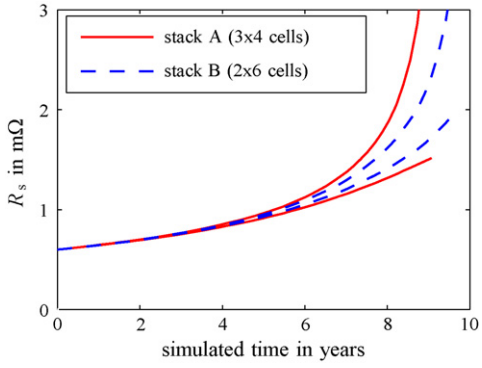

Fig. 16. Comparison of the development of the series resistance in the two stack designs. For each stack A and B the resistance of the worst and the best cell is shown, respectively.

that stack A exhibits a stronger dispersion. Cells 4–9 become warmer, because they have less contact to the surroundings.

Fig. 16 shows the development of the series resistance of the best and the worst cell for both stack designs. While the difference during the first years is marginal, stack B exhibits less dispersion at an advanced ageing state. While the temperature distribution provides some information about the reason for the dispersion, the ageing simulation and analysis of the model parameters allows assessing its influence on the performance and life expectancy of the cells.

3. Conclusion

The simulation results of the holistic ageing model show that self-accelerating deterioration effects can lead to significant divergence of cell characteristics and finally to the failure of individual cells. Two important conclusions can be drawn from the simulations: firstly, temperature inhomogeneities in a stack can lead to significant decrease of life expectancy. Secondly, as soon as a cell has approximately doubled its resistance, its further degradation is strongly accelerated and will soon make the whole stack inoperable, if no countermeasures are taken.

We would like to emphasise, that the absolute numbers regarding life expectancy or cell performance after a certain ageing time have to be interpreted with great care. Since the system includes positive feedback loops, it is sensitive to relatively small errors in each of the model parts. From the assumptions discussed in Section 2.4 the extrapolation to low voltages and temperatures is probably the most critical one. Kötz et al. have extrapolated life expectancies of more than 10 years at 2.5 V and 65 ° C from leakage current measurements [16]. The results of the measurements presented in Part I [1]– though carried out on different devices – do not support this optimistic prognosis, but might also lead to over- or underestimation of the ageing behaviour if extrapolated far from the test conditions. Further research for a better understanding of the physical and chemical processes involved in the ageing process will help to improve the absolute accuracy and validity range of the model.

The holistic EDLC model nevertheless is a valuable tool for studying the influence of stack design, thermal management, operating strategies, cell balancing and the like on the life expectancy of each individual cell. For the development of EDLC storage systems different designs and operating modes can be compared and benchmarked with respect to performance and life expectancy.

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